

On the Origin of Charging Damage during Etching of Antenna Structures

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ABSTRACT

Monte Carlo simulations of charging and profile evolution in patterned antenna structures during etching in high-density plasmas reveal a rapid change in the potential of the lines at end point, which causes a surge in electron tunneling through thin gate oxides and possibly charging damage. The condition of the substrate (grounded vs. floating) determines the magnitude of the surge and whether it will be followed by a steady-state current until all lines of the pattern become disconnected. A reduction in damage is possible by controlling the substrate condition, which may be assessed through notching experiments.

When plasma-etching patterned wafers, the directionality difference between ions and electrons at the wafer causes differential microstructure charging,¹ which affects the in-trench etch rate,² can lead to profile distortion (notching),^{3,4} and may induce electron tunneling through thin gate oxides.^{1,5} Large tunneling currents are believed to cause electrical degradation or even breakdown of the oxide.⁶ Termed the "electron shading" effect,¹ this form of damage is particularly aggravating because of its latent nature and is feared to become a showstopper in the quest for smaller critical dimensions. Despite tremendous effort by researchers worldwide to fight the problem,⁷ a solution has yet to be found. The physics of the electron shading damage has been elusive, in part because of the experimental hurdles in measuring tunneling currents *in situ* under realistic processing conditions.

Numerical simulations could provide insight into the origin of the tunneling currents and improve understanding of the limitations of existing etch tools and device layout rules. To be sure, such simulations are complex; the charging and etching processes are coupled, requiring the simultaneous handling of phenomena that occur over disparate time scales such as electron tunneling ($<10^{-7}$ s), microstructure charging (10^{-3} s), and profile evolution (10^2 s), on patterned surfaces consisting of dissimilar materials. Results from such comprehensive calculations for gate electrode etching suggest that the period from open area clearing (end point) to trench bottom clearing is critical for damage.^{5,8} Tunneling current transients occur during that time, albeit with peak currents that may not be large enough to cause breakdown of the gate oxide. Cumulative charge damage was found only under edge gates, in patterns separated by open areas covered with field oxide.⁵

Here we focus on tunneling current transients in patterned antenna structures; being area intensive, antennas amplify the ion and electron current imbalance and can force large tunneling currents through small area gate oxides.¹ We are aware of only one prior simulation effort by Kinoshita *et al.*,⁹ who studied current injection during etching of metal antenna structures by performing steady-state charging calculations; since the profile evolution was not simulated, no true current transients could be captured. Krishnan *et al.*¹⁰ reported that, in the presence of aspect ratio dependent etching (ARDE),¹¹ damage "occurs exclusively during clearing of the metal (end point)." Kinoshita *et al.*⁹ argued that a large steady-state tunneling current flows through the gate oxide from end point until the metal in trench bottoms clears, causing the damage. For an antenna ratio of 16,000:1, the steady-state current was calculated to be 7.20 A/cm². Interestingly, the potential difference across the 3.5 nm gate oxide was 6.1 V, assuming grounded substrate. The numbers correspond to an oxide field of $(6.1/3.5 =) 1.743$ V/nm or 17.43 MV/cm, significantly above the threshold of 12 MV/cm for instantaneous oxide breakdown,⁶ and therefore questionable.^a

We simulate etching under conditions identical to those used by Kinoshita *et al.*,⁹ namely, a plasma density of 4.5×10^{10} cm⁻³, electron temperature of 1.25 V, ion temperature of 0.1 V. The wafer electrode is biased at 13.56 MHz with a peak-to-peak voltage of 100 V. The pattern consists of five isolated 0.5 μ m lines separated by 1.0 μ m spaces (trenches). Identical patterns are separated by large open areas. At the onset of etching, each feature consists of a 1.0 μ m photoresist mask onto a layer of 0.8 μ m n⁺-poly-Si, formed on

top of a thick (>100 nm) layer of SiO₂. One line sits on top of a poly-Si conduit to a small area covered by 3.5 nm gate oxide (antenna structure, Fig. 1). The antenna ratio is taken to be 16,000:1. We chose to etch poly-Si in a chlorine plasma because validated models of plasma-surface interactions exist for this system.⁴

The Monte Carlo simulations of microstructure charging and profile evolution are performed as described elsewhere.⁴ Electron tunneling currents through thin gate oxides are accounted for, explicitly and self-consistently.^{5,8} In addition, the simulation couples sheath dynamics, charge particle dynamics, topography charging, surface chemistry, and scattering effects. Tunneling current transients would not occur without ARDE;⁵ the simulation describes ARDE solely as a result of differential charging, while neutral shadowing¹¹ is not important in the ion-limited etching regime considered here. Since the aspect ratio is low (1:1 at the start, 1.8:1 at the end of etching), the difference in etch rate between the trenches and the open area is small. We calculated a difference of about 3.2%, which implies a short initial overetch to clear the latent antenna. Because of the low aspect ratio, the profile evolves with relatively straight sidewalls and flat bottom.

When monitoring tunneling currents, the substrate potential plays a central role, given that the potential difference across the oxide determines whether tunneling will occur, the polarity of the current, and its magnitude. A grounded substrate is clearly an extreme that is difficult to realize in practice,⁶ although it simplifies the calculations considerably. The other extreme is that of a floating substrate, completely isolated from the plasma and capable of responding immediately to current injections. For completeness, both cases are considered.

We begin by monitoring the potential of various lines (V_i , $i = A, B, C$) and the substrate (V_{sub}), during various phases of the etch (Table I). During the main etch, all potentials are at zero. As soon as the open area clears, the potential of the connected lines jumps up to a new value, which remains constant during the initial overetch, until the trench bottoms become disconnected. In the next phase (the final overetch), the potentials of the lines change individually, but not independently.¹² Since there is not much re-entrant sidewall left to collect ions (*vide supra*), the potentials do not vary much as the final overetch progresses.

The changes in the potentials with etch time occur because of variations in the supply of electrons to the lines as the profile evolves, and can be understood in conjunction with the tunneling

^a The substrate is "grounded" when its potential remains constant despite the current injection. This situation occurs when large "patches" of substrate are directly (or through a thin oxide) exposed to the plasma, e.g., at wafer edges, at scribe lines (separating dies), or at open areas separating dense patterns.

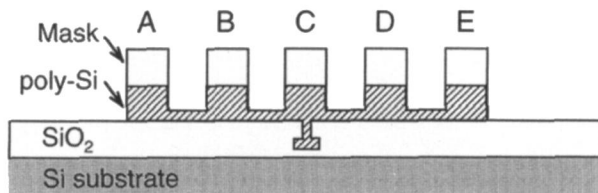


Fig. 1. Schematic of the antenna structure as it would be at end point.

^a The oxide field should exceed threshold (12 MV/cm) for catastrophic failure of the oxide. However, the exponential dependence of the tunneling current on oxide field poses limitations to how much above the threshold one can go before the the 3.5 nm oxide is vaporized away (see Ref. 6, p. 449).

Table I. Steady-state potentials of various lines and the substrate during the two phases of the overetch.

Potential (V)	Floating substrate		Grounded substrate	
	Initial overetch	Final overetch	Initial overetch	Final overetch
V_A	16.20	10.00	4.98	7.50
V_B	16.20	24.90	4.98	22.50
V_C	16.20	24.95	4.98	4.64
V_{sub}	12.98	22.05	0	0

current, plotted in Fig. 2. During the main etch, no tunneling current flows. The ion and electron current imbalance at the patterned area is compensated for by electrons bombarding the open area (unshaded). When the open area clears, electrons can only be supplied to the outer edge of the pattern. The potential of the connected lines must increase to attract more electrons, so that the balance is maintained. As the substrate attempts to follow (floating case), electrons tunnel to the poly-Si giving rise to the 1st transient (Fig. 2a), with more than 1 A/cm² surging through the gate oxide. Tunneling stops when the potential of the lines reaches a value high enough to (i) deflect a number of low energy ions in the patterned area and (ii) attract more electrons at the outer edge of the pattern, so that current equality to the latent antenna is re-established. The current balance is perturbed one more time, when the lines become disconnected. The electron supply to the outer edge of line A becomes localized and decreases V_A . V_B and V_C must increase to deflect more ions; as V_{sub} trails, a second current transient appears, albeit of a smaller magnitude. We emphasize that these are true transients, controlled by rapid charging.

When the substrate is grounded, the picture changes dramatically (Fig. 2b). The first current transient reaches almost 3 A/cm², before dropping to a steady-state value of 2.3 A/cm², which lasts throughout the initial overetch. Since the potential of the connected lines does not rise as much as in the previous case (Table I), fewer electrons are attracted at the outer edge of the pattern. Thus, more substrate electrons must tunnel to balance the ion current. As soon as the lines become disconnected, the current drops to 0.55 A/cm², where it remains throughout the final overetch. Note

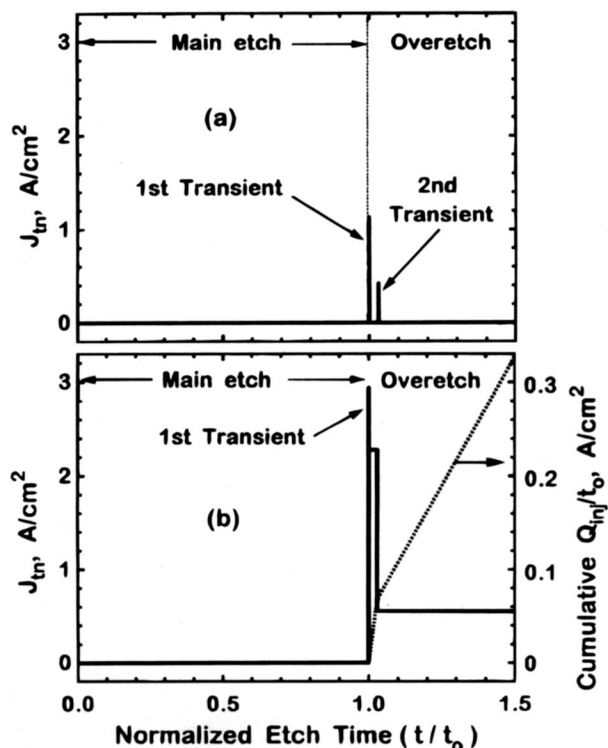


Fig. 2. The tunneling current through the gate oxide as a function of the normalized etch time, for (a) floating and (b) grounded substrate. t_0 is the duration of the main etch. The cumulative charge over time is also shown for (b).

that the cumulative damage may now become noticeable. Assuming a 3 s initial overetch, the cumulative charge injected (Q_{inj}) is only 0.21 C/cm², which is two orders of magnitude smaller than that calculated by Kinoshita *et al.*⁹ The total Q_{inj} increases with overetch time, but more than 50% overetch is required before it reaches 20 C/cm².

Our results clearly suggest that the first current transient is responsible for damage. When the substrate is grounded,⁶ the oxide field peaks at 14.23 MV/cm, causing instantaneous oxide breakdown (C-mode failure);⁶ the sustained high current during the initial overetch can only worsen damage. When the substrate is floating, the oxide field peaks at 9.20 MV/cm, exceeding the B-mode failure threshold.⁶ In both cases, the damage occurs probably because a large tunneling current surges through the thin oxide. The timing of the surge coincides with when the damage is observed experimentally.¹⁰

How can current transients be suppressed? Since their occurrence is inextricably linked to ARDE, control of the latter may appear to be the answer. Unfortunately, ARDE is a consequence of differential charging when etching is ion-limited^{5,8} and, thus, it is impossible to eliminate without attacking the problem of differential charging itself. Based on the results presented, we propose another approach that exploits the role of the substrate potential. Since an antenna structure on a grounded substrate suffers most of the

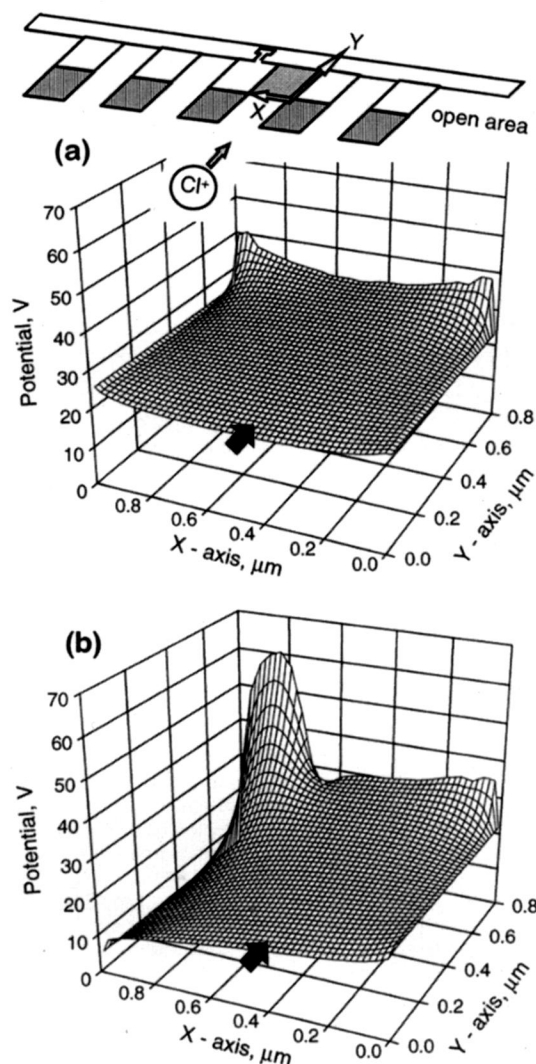


Fig. 3. Three-dimensional charging potential distributions in the trench area next to the middle line for (a) floating and (b) grounded substrate. The inset illustrates the area of interest and defines the origin for the potential surface. The microstructure has been rotated to allow for a more convenient description of ion motion in the trench. The arrows show the direction of ions as they approach the potential surface.

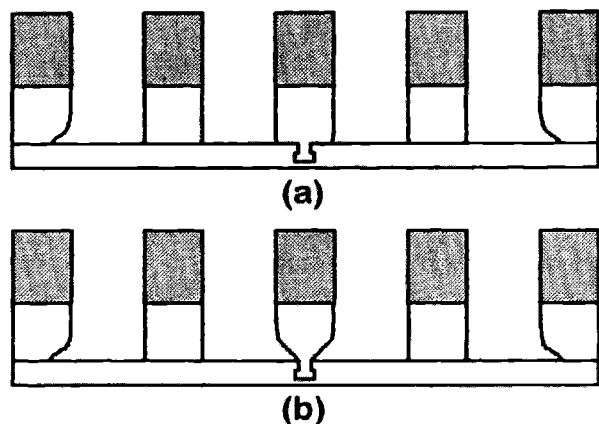


Fig. 4. Simulated notch profiles at the sidewalls of the various lines after 100% overetching for (a) floating and (b) grounded substrate. Etching of the outer sidewalls of the edge lines is not simulated. The aspect ratio has been preserved.

damage, elimination of all reasons for pinning the substrate potential low⁵ could significantly reduce the magnitude of the transient current.

But in today's complex chip designs, how can one assess the condition of the substrate? There is actually a simple test one can perform, based on the occurrence of notching at the sidewalls of the line connected to the thin oxide (middle line). In the absence of sidewall passivation, overetching a structure like that of Fig. 1 will cause notching at the inner side of the edge lines (classic notching).⁴ If the substrate is floating, notching occurs nowhere else, as the potential of no other line is low (Table I). However, if the substrate is grounded, the potential of the middle line is actually lower than that of the edge line since more electrons arrive by tunneling through the thin oxide. As a result, notching will occur at both sidewalls of the middle line and, in fact, it will be deeper than that at the edge line. The degree by which the two notches differ is a strong function of the substrate area directly exposed to the plasma.

These ideas can be better understood by examining the charging potentials in the trench next to the middle line. In the case of a floating substrate (Fig. 3a), the potential surface has a very small peak next to the sidewall foot of the middle line. Only very low energy ions will be affected by it. In contrast, when the substrate is grounded (Fig. 3b), the peak is huge and the perturbation in the trajectories of all but the most energetic ions approaching this potential wall will be very significant. The distribution has the "classic" asymmetric shape that leads to severe notching.⁴ Indeed, the

profile evolution simulation quantifies these claims. The results are compared in Fig. 4, where symmetric notches appear at the sidewalls of the middle line only for the grounded substrate; as predicted, these notches are deeper than those occurring at the edge lines of the same structure.

In conclusion, simulations of charging and profile evolution during plasma etching suggest that charging damage in antenna structures may ensue as a result of tunneling current transients surging through thin gate oxides at end point, which may be followed by large steady-state currents until the lines in patterned areas become disconnected. The substrate's role in tunneling may be exploited to minimize the surge maximum and eliminate the steady-state current during the initial overetch, which should help decrease charging damage.

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